

Appl. No. 09/976,522

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (original): A multi-service segmentation and reassembly (MS-SAR) integrated circuit, comprising:

- a first bus interface;
- lookup circuitry;
- segmentation circuitry;
- reassembly circuitry;
- a second bus interface; and

a data path extending from the first bus interface to the lookup circuitry, and from the lookup circuitry to the segmentation circuitry, and from the segmentation circuitry to the reassembly circuitry, and from the reassembly circuitry to the second bus interface, wherein both cell-protocol traffic and packet-protocol traffic pass over the data path from the first bus interface, through the lookup circuitry, through the segmentation circuitry, through the reassembly circuitry and out of the integrated circuit from the second bus interface, the lookup circuitry analyzing the cell-protocol traffic and outputting information that causes the cell-protocol traffic to be processed in a first way by the segmentation circuitry and the reassembly circuitry, the lookup circuitry analyzing the packet-protocol traffic and outputting information that causes the packet-protocol traffic to be processed in a second way by the segmentation circuitry and the reassembly circuitry.

Claim 2 (original): The integrated circuit of Claim 1, wherein the integrated circuit is operable in a first ingress mode such that traffic is output from the integrated circuit to a cell-based switch fabric via the second bus interface, and wherein the integrated circuit is operable in a second ingress mode such that traffic is output from the integrated circuit to a packet-based switch fabric via the second bus interface.

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Claim 3 (original): The integrated circuit of Claim 1, wherein the integrated circuit is operable in a first egress mode such that traffic is received onto the integrated circuit from a cell-based switch fabric via the first bus interface, and wherein the integrated circuit is operable in a second egress mode such that traffic is received onto the integrated circuit from a packet-based switch fabric via the first bus interface.

Claims 4 to 5 (cancelled)

Claim 6 (original): The integrated circuit of Claim 1, wherein the cell-protocol traffic is ATM traffic, and wherein the packet-protocol traffic is MPLS traffic.

Claim 7 (original): The integrated circuit of Claim 1, further comprising:  
memory manager circuitry, wherein the data path extends from the segmentation circuitry to the reassembly circuitry via the memory manager circuitry.

Claim 8 (original): The integrated circuit of Claim 1, wherein the cell-protocol traffic involves an ATM cell, and wherein the packet-protocol traffic involves a packet, the ATM cell being temporarily stored in one of a plurality of buffers of a memory, all of the buffers being of equal size, the packet being segmented into a plurality of chunks, and each of the chunks being temporarily stored into a corresponding one of the buffers.

Claim 9 (currently amended): An integrated circuit comprising:

- a first bus interface;
- means for generating a segmentation trailer;
- means for checking a segmentation trailer;
- a second bus interface; and
- a data path extending from the first bus interface to the means for generating, and from the means for generating to the means for checking, and from the means for checking to the second bus interface, wherein both cell-protocol traffic and packet-protocol traffic pass over the data path from the first bus interface, through the means for generating, through the means for checking, and out of the integrated circuit from the second bus interface.

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Claims 10 to 44 (cancelled)

Claim 45 (previously presented): An integrated circuit, comprising:  
a first bus interface;  
a second bus interface adapted for coupling to a switch fabric; and  
means for receiving network information from the first bus interface, a first portion of the network information being received in a cell-protocol, a second portion of the network information being received in a packet-protocol, the means also being for passing the network information through a single data path from the first bus interface and to a payload memory and then through the single data path from the payload memory and to the second bus interface.

Claim 46 (previously presented): The integrated circuit of Claim 45, wherein the payload memory is a memory external to the integrated circuit.

Claim 47 (previously presented): The integrated circuit of Claim 45, wherein the means includes a segmentation engine, the segmentation engine being controlled to process the first portion of network information in a first way and to process the second portion of network information in a second way.

Claim 48 (previously presented): The integrated circuit of Claim 45, wherein the means includes a reassembly engine, the reassembly engine being controlled to process the first portion of network information in a first way and to process the second portion of network information in a second way.

Claim 49 (previously presented): An integrated circuit, comprising:  
a first bus interface adapted for coupling to a switch fabric;  
a second bus interface; and  
means for receiving network information from the switch fabric via the first bus interface, a first portion of the network information being received in a cell-protocol, a second portion of the network information being received in a packet-protocol, the means also being for passing the network information through a single data path from the first bus interface and to a payload

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memory and then through the single data path from the payload memory and to the second bus interface.

Claim 50 (previously presented): The integrated circuit of Claim 49, wherein the payload memory is a memory external to the integrated circuit.

Claim 51 (previously presented): The integrated circuit of Claim 49, wherein the means includes a segmentation engine, the segmentation engine being controlled to process the first portion of the network information in a first way and to process the second portion of the network information in a second way.

Claim 52 (previously presented): The integrated circuit of Claim 49, wherein the means includes a reassembly engine, the reassembly engine being controlled to process the first portion of the network information in a first way and to process the second portion of the network information in a second way.

Claim 53 (previously presented): A method, comprising:

receiving network information on a first bus interface of an integrated circuit, a first portion of the network information having a cell-protocol as it is received onto the integrated circuit, a second portion of the network information having a packet-protocol as it is received onto the integrated circuit;

passing the network information through a single data path from the first bus interface, through a segmentation engine of the integrated circuit, and to a payload memory and then through the single data path from the payload memory, through a reassembly engine of the integrated circuit, and to a second bus interface of the integrated circuit;

processing the first portion of the network information in a first way as it passes through the single data path; and

processing the second portion of the network information in a second way as it passes through the single data path.